Amendments to the Claims

Please amend the claims in the manner indicated.

1. (currently amended) A method for storing data in a cache comprising:

prioritizing a locked way of the cache higher than a recently used way; and

prioritizing an additional locked way higher than the locked way.

2. (original) The method of claim 1, further comprising storing data in the recently used way.

3. (original) The method of claim 1, further comprising:

prioritizing the locked way higher than a least recently used way; and

storing data in the least recently used way.

4. (original) The method of claim 1, further comprising locking at least one way of the cache to provide the locked way.

5. (original) The method of claim 1, further comprising reading data from a way of the cache prior to prioritizing the locked way, the way being the recently used way.

6. (original) The method of claim 1, wherein prioritizing the locked way includes setting a bit in a register.

7. (original) The method of claim 1, further comprising setting a bit in a register to indicate priority of the recently used way.

8. (original) The method of claim 1, further comprising writing data to a way of the cache prior to prioritizing the locked way, the way being the recently used way.

9-10. (cancelled)

11. (currently amended) The method of claim 1 [[9]] , further comprising:

setting a first bit in a register to indicate priority of the locked way; and

setting a second bit in a register to indicate priority of the additional locked way.

12. (original) The method of claim 11, further comprising setting a third bit in a register to indicate priority of the recently used way.

13. (currently amended) A method comprising:

locking a first way of a cache;

locking ~~accessing~~ a second way of the cache;

accessing a third way of the cache; and

prioritizing the first way of the cache higher than the second way of the cache [[;]] ~~and writing data to the second way of the cache~~.

14. (previously presented) The method of claim 13, wherein locking the first way includes setting a bit in a register to indicate the priority of the first way.

15-16. (cancelled)

17. (currently amended) An apparatus comprising a cache having a first way and a second way, the apparatus comprising:

a circuit adapted to lock the first way and the second way and to prioritize the first locked way higher than the second locked way ~~write data to the first way if the first way has been accessed more recently than the second way~~.

18. (cancelled)

19. (currently amended) The apparatus of claim 17, further comprising a memory location adapted to indicate the priorit[[y]]ies of the first way and the second way.

20-22. (cancelled)